

**Notice of References Cited**Application/Control No.  
09/483,321Applicant(s)/Patent Under  
Reexamination  
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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,378,090 ✓	04-2002	Bhattacharya, Debasish	712/38
	B	US-6,446,230 ✓	09-2002	Chung, Sung Soo	714/726
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Landis, D.L.; Singh, P., "Optimal placement of IEEE 1149.1 test port and boundary scan resources for wafer scale integration," Proceedings of the International Test Conference, 1990 Pages: 120 -126 ✓
	V	Fitch, K.D.; Kane, J., "Application of boundary-scan and full-chip BIST to a 3 ASIC chip set," Proceedings of the IEEE 1991 Custom Integrated Circuits Conference, 1991, Pages: 17.5/1 -17.5/4. ✓
	W	Andrews, J., "An embedded JTAG, system test architecture," Electro/94 International Conference Proceedings. Combined Volumes, 199, Page(s): 691 -695. ✓
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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